## REMARKS

Claims 1-22 are pending and under consideration.

### STATEMENT ON SUBSTANCE OF INTERVIEW

An in-person interview was conducted between the Applicant's representative and the Examiner on January 21, 2005. During the interview, the Applicants' representative pointed out that previously filed arguments were not addressed by the Examiner in the current Action, claim 2 as written is not indefinite, and the cited art does not teach features recited in the claims. Other points raised at the interview are included below.

Regarding the Examiner's question on a flow of FIG. 4, the attention of the Examiner is directed to pages 15 starting at line 12 which discusses that FIG. 4 shows "in this second embodiment, the noise countermeasures determined by the first embodiment are further optimized." (Emphasis added).

Applicants thanks the Examiner for the opportunity to conduct an in-person interview.

### ITEMS 20-22: REJECTION OF CLAIM 2 UNDER 35 U.S.C. §112, ¶2

In items 20-22, the Examiner rejects claim 2 under U.S.C. §112, second paragraph as indefinite contending the term "categorizing the noise" is not adequately defined. (Action at page 4). In items 11-12, the Examiner requests clarification of the term and contends that since the definition submitted by the Applicant in the Amendment filed August 4, 2004, was:

> not (from) a technical dictionary, and "categorizing the noise" appears to be a technical term . . . The Examiner will carefully consider any references supplied by the Applicant in the future that support this assertion.

(Action at pages 2-3).

As discussed during the in-person interview, the term "categorizing," itself, is not a technical term and that the action of observing features, whatever those features may be, and "categorizing" in accordance with the features is understood in the art as a basic educational concept.

Further, claim 2 recites "carrying out a circuit simulation using the simulation model, to calculate a signal waveform propagating through a wiring of the target circuit and to check whether or not a noise exceeding a tolerable range exists in the signal waveform; and categorizing the noise existing as a result of the noise check, and optimizing the determined noise countermeasures to only portions related to the noise." That is, the "categorizing" is based on "whether or not a noise exceeding a tolerable range exists in the signal waveform."

For example, while it is difficult to know the cause of the noise solely from the signal waveform, it is easier to know from the noise countermeasure the level (voltage) and the timing

(noise generation time) of the noise that is generated when this noise countermeasure is not taken, and it is therefore easy to categorize the noise into the noise that is seen in the simulation result and the noise that is not seen in the simulation result.

Further, it is understood in the art that categorizing is a common verb. For example, the Computer, Telephony & Electronic Industry Glossary indicates "To categorize; to set apart various items into groups with similar characteristics." (See, http://www.csgnetwork.com/glossarys.html).

Applicants submit that claim 2 complies with 35 U.S.C. §112, second paragraph and request withdrawal of the rejection.

**ITEMS 30-48: REJECTION OF CLAIMS 1-3, 7-9 AND 21-22 AS ANTICIPATED BY TSUCHIDA (U.S.P. 5,559,997)**

The Examiner rejects independent claims 1 (and dependent claims 2-3, 7-9, and 21-22) as anticipated by Tsuchida citing Tsuchida's FIG. 1 and abstract. In item 14, page 3 the Examiner cites Tsuchida FIG 1 element 2103, the looping path through 2103, 2104, 2105, 2106, 2107, 2109, and 2103 as teaching the feature of determined.

Independent claim 1 recites a noise countermeasure determination method "calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures."

**Features Not Taught By Tsuchida**

As discussed during the in-person interview, Tsuchida does not teach how noise countermeasures are determined based on calculating recommended circuit information, and does not teach comparing input circuit information and the recommended circuit information, so as to determine the noise reduction components (noise countermeasures).

Tsuchida merely teaches designing a printed-circuit board based on the "fundamental circuit design" and the "noise reduction components (or noise countermeasures)" that are input. (See, for example, col. 3. starting at line 10). The looping path cited by the Examiner does not teach determining noise countermeasures based on calculating recommended circuit information, but merely is a general PCB design procedure.

For example, problems discussed in the specification (see, for example page 4, lines 30-34 in which noise countermeasures are determined to be too sever and require a damping

resistor to be modified) that are addressed by the present invention, are still encountered in methods as taught by Tsuchida.

**Conclusion**

Since Tsuchida does not describe features in recited in claims 1-3, 7-12, and 16-22, the rejection should be withdrawn, and claims 1-3, 7-9, and 20-22 allowed.

**ITEMS 49: REJECTION OF CLAIMS 10-12 AND 16-18 UNDER 35 U.S.C. §102(b) AS ANTICIPATED BY TSUCHIDA**

The Examiner rejects independent claim 10 (and claims 11-12 and 16-18) for the same reasons as the rejection of independent claim 1 (and claims 2-3 and 7-9 respectively). (Action at page 8).

Independent claim 10 recites a noise countermeasure determination apparatus including "a recommended circuit information calculating section calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and a noise countermeasure determination section comparing the input circuit information and the recommended circuit information, and determining a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures." (Emphasis added).

**Features Not Taught By Tsuchida**

As discussed during the in-person interview Tsuchida does not teach calculating recommended circuit information, comparing input circuit information and the recommended circuit information, so as to determine the noise countermeasures. Tsuchida merely teaches a method of designing a printed-circuit board based on the "fundamental circuit design" and the "noise reduction components (or noise countermeasures)" that are input. (See, for example, col. 3. starting at line 10).

**Conclusion**

Since features recited in independent claim 10 (and claims 11-12 and 16-18) are not taught by the cited art, the rejection should be withdrawn, and claims 10-12 and 16-18 allowed

**ITEM 50: REJECTION OF CLAIM 19 UNDER 35 U.S.C. §102(b) AS ANTICIPATED BY TSUCHIDA**

The Examiner rejects independent claim 19 for the same reasons as the rejection of claim 1. (Action at page 8).

Independent claim 19 recites a computer-readable storage storing a program for

controlling a computer to determine noise countermeasures, by "calculating recommended circuit information considered to minimize a noise by use of at least one formula, based on input circuit information amounting to at least one net of a target circuit which is to be subjected to a noise analysis; and comparing the input circuit information and the recommended circuit information, and to determine a differing portion of the recommended circuit information differing from the input circuit information, as noise countermeasures." (Emphasis added).

**Features Not Taught By Tsuchida**

As discussed during the in-person interview, Tsuchida does not teach calculating recommended circuit information, comparing input circuit information and the recommended circuit information, so as to determine the noise countermeasures. Tsuchida merely teaches a method of designing a printed-circuit board based on the "fundamental circuit design." (See, for example, col. 3. starting at line 10).

**Conclusion**

Since features recited in claim 19 are not taught by the cited art, the rejection should be withdrawn, and claim 19 allowed.

**ITEMS 54-58, 68: REJECTION OF CLAIMS 4 AND 13 UNDER 35 U.S.C. §103(a) OVER TSUCHIDA IN VIEW OF DORF (THE ELECTRICAL ENGINEERING HANDBOOK, SECOND EDITION, RICHARD C. DORF, EDITOR CRC PRESS, 1997)**

The Action concedes that Tsuchida does not teach a method:

> . . . compares(ing) a damping resistance which makes a voltage at a time of a ringback equal to the minimum voltage VIH-1 and the minimum value of the damping resistance, and outputs(ing) a larger one of the damping resistance.

(Action at page 9). Nevertheless, the Examiner rejects claims 4 and 13 under 35 U.S.C. §103(a) as unpatentable over Tsuchida in view of Dorf. (Action at pages 9 and 11). These rejections are identical to those in the previous Office Action.

As Applicants aruged in the Amendment filed August 4, 2004, the Examiner has not supported his contention regarding implicit teachings of Tsuchida. As set forth in MPEP §707.07(f) entitled Answer All Material Traversed:

> an examiner must provide clear explanations of all actions taken by the examiner during prosecution of an application.

Applicants submit that the finality of the present rejection should be withdrawn since the Office Action is incomplete, and the Examiner has not responded to the Applicants argument other than to repeat the Examiner's contentions from the previous Action and that do not address the Applicants' arguments.

**Conclusion**

Since the Examiner's contentions are unsupported, and the Office Action is incomplete, the rejection should be withdrawn and claims 4 and 13 allowed.

**ITEMS 53-55, 60-61: REJECTION OF CLAIMS 5 AND 14 UNDER 35 U.S.C. §103(a) UNDER 35 U.S.C. §103(A) OVER TSUCHIDA IN VIEW OF GUO (U.S.P. 6,597,808).**

The Action concedes that Tsuchida does not teach recited features of :

> . . . outputting the input circuit information which includes, as a wiring length, a Manhattan distance which is determined based on positions of part pins forming the target circuit and a wiring topology.

(Action at page 8). Nevertheless, the Examiner rejects claims 5 and 14 under 35 U.S.C. 103(a) as being unpatentable over Tsuchida in view of Guo. (Action at pages 8-9 and page 10). These rejections are identical to those in the previous Office Action.

As discussed during the in-person interview and as Applicants argued in the Amendment filed August 4, 2004, the Examiner has not supported his contention of Tsuchida's implicit teachings.

Applicants submit that the finality of the present rejection should be withdrawn since the Office Action is incomplete, and the Examiner has not responded to the Applicants' argument other than to repeat the Examiner's contentions from the previous Action and that do not address the Applicants' arguments.

**Conclusion**

Since the Examiner's contentions are unsupported, and the Office Action is incomplete, the rejection should be withdrawn and claims 4 and 13 allowed.

**ITEMS 56-61: REJECTION OF CLAIMS 6 AND 15 UNDER 35 U.S.C. §103(a) OVER TSUCHIDA IN VIEW OF GUO**

The Examiner rejects claim 6 under 35 U.S.C. 103(a) as being unpatentable over Tsuchida in view of Guo. (Action at page 9). The Examiner rejects claim 15 for the same reasons as the rejection of claim 6. (Action at page 10).

Claims 6 and 15 recite, respectively, a noise countermeasure determination method and apparatus, using claim 6 as an example, "determining an optimum wiring topology from results of the noise check carried out in said carrying out a circuit simulation using the simulation model to use in said outputting input circuit information so that the optimum wiring topology is determined as the noise countermeasures in said comparing the input circuit information and the recommended circuit information." (Emphasis added).

Applicants submit that the cited art, alone or in combination, does not teach determining an optimum wiring topology.

The Examiner contends that the "iterative loop in Tsuchida FIG. 1 is an optimizing iterative loop. However, Tsuchida merely teaches (see, for example, col. 1 starting at line 30 that FIG. 1 teaches related art in which a designer examines whether the "whether the PC board operates as is expected."

**Conclusion**

Since features of claims 6 and 15 are not taught by the cited art and *prima facie* obviousness is not established, the rejection should be withdrawn and claims 6 and 15 allowed.

## CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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